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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
STOYNOV, STEFAN	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/027,392	COOPER, BARNES	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *21 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,9-13,19-23,29 and 30* is/are rejected.

7)☒ Claim(s) *4-8,14-18 and 24-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 9-13, 19-23, 29, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura.

Re claim 1, Nakamura discloses a method comprising:

- determining a processor state of a processor (column 2, line 45-54) upon expiration of a system management interrupt (SMI) timer (column 8, lines 52-55), the processor state being one of an operational sate (column 6, line 1-4) and a low power state (column 6, lines 7-10);
- loading the SMI timer with a timer value (column 8, lines 23-28) based on the processor state, the timer value being one of a first value and a second value (FIG. 11C, T1 and T2); and
- transitioning the processor to one of the operational sate and the low power state according to the processor state (FIG. 11B).

Re claim 2, Nakamura discloses the method wherein loading the SMI timer comprises:

- loading the SMI timer with first value (column 17, line 67, column 18, lines 1-6, and FIG. 11C, T2) if the processor state is the operational state (FIG. 11B); and

- loading the SMI timer with the second value (column 18, lines 18-30 and FIG. 11C, T1) if the processor sate is the low power state (FIG. 11B).

Re claim 3, Nakamura discloses the method wherein transitioning comprises:

- transitioning the processor to the operational state if the processor state is the low power state (FIG. 11B); and
- transitioning the processor to the reduced power state if the processor is operational state (FIG. 11B).

Re claim 9, Nakamura discloses the method wherein transitioning the processor to the low power state comprises:

- transitioning the processor to a sleep state (column 6, lines 34-39 and FIG. 2).

Re claim 10, Nakamura discloses the method wherein loading the SMI timer comprises:

- loading the SMI timer in a chipset (column 7, lines 10-13, gate array defined as chip in Microsoft Computer Dictionary, Fifth Edition).

Re claim 11, Nakamura discloses a computer program product (column 6, lines 62-67) comprising a machine usable medium having computer program code embedded therein, the computer program product having:

- computer readable program code to determine a processor state of a processor (column 2, line 45-54) upon expiration of a system management interrupt (SMI) timer (column 8, lines 52-55), the processor state being

one of an operational state (column 6, line 1-4) and a low power state (column 6, lines 7-10);

- computer readable program code to load the SMI timer with a timer value (column 8, lines 23-28) based on the processor state, the timer value being one of a first value and a second value (FIG. 11C, T1 and T2); and
- computer readable program code to transition the processor to one of the operational state and the low power state according to the processor state (FIG. 11B).

Re claim 12, Nakamura discloses the computer program product wherein the computer readable program code to load the SMI timer comprises:

- computer readable program code to load the SMI timer with the first value (column 17, line 67, column 18, lines 1-6, and FIG. 11C, T2) if the processor state is the operational state (FIG. 11B); and
- computer readable program code to load the SMI timer with the second value (column 18, lines 18-30 and FIG. 11C, T1) if the processor state is the low power state (FIG. 11B).

Re claim 13, Nakamura discloses the computer program product wherein the computer readable program code to transition comprises:

- computer readable program code to transition the processor to the operational state if the processor state is the low power state (FIG. 11B); and

- computer readable program code to transition the processor to the reduced power state if the processor state is the operational state (FIG. 11B).

Re claim 19, Nakamura discloses the computer program product wherein the computer readable program code to transition the processor to the low power state comprises a sleep state (column 6, lines 34-39 and FIG. 2).

Re claim 20, Nakamura discloses the computer program product wherein the computer readable program code to load the SMI timer comprises:

- computer readable program code to load the SMI timer in a chipset (column 7, lines 10-13, gate array defined as chip in Microsoft Computer Dictionary, Fifth Edition).

Re claim 21, Nakamura discloses a computer system comprising:

- a processor (FIG. 1, 11);
- a memory coupled to the processor (FIG. 1) to store the throttling emulator (column 7, lines 28-32, column 7, lines 38-42), the throttling emulator, when executed, causing the processor to:
  - determine a processor state of the processor (column 2, line 45-54) upon expiration of a system management interrupt (SMI) timer (column 8, lines 52-55), the processor sate being one of an operational state (column 6, line 1-4) and a low power state (column 6, lines 7-10);

- load the SMI timer with a timer value based on the processor state, the timer value being one of a first value and a second value (FIG. 11C, T1 and T2); and
- transition the processor to one the operational state and the low power state according to the processor state (FIG. 11B).

Re claim 22, Nakamura discloses the system wherein the throttling emulator causing the processor to load causes the processor to:

- load the SMI timer with the first value (column 17, line 67, column 18, lines 1-6, and FIG. 11C, T2) if the processor state is the operational state (FIG. 11B); and
- load the SMI timer with the second value (column 18, lines 18-30 and FIG. 11C, T1) if the processor sate is the low power state (FIG. 11B).

Re claim 23, Nakamura discloses the system wherein the throttling emulator causing the processor to transition causes the processor to:

- transition the processor to the operational state if the processor state is the low power state (FIG. 11B); and
- transition the processor to the reduced power state if the processor state is the operational state (FIG. 11B).

Re claim 29, Nakamura discloses the system wherein the throttling emulator causing the processor to:

- transition the processor to the low power state causes the processor to transition to a sleep state (column 6, lines 34-39 and FIG. 2).

Re claim 30, Nakamura discloses the system wherein the throttling emulator causing the processor to load the SMI timer causes the processor to:

- load the SMI timer in a chipset (column 7, lines 10-13, gate array defined as chip in Microsoft Computer Dictionary, Fifth Edition).

Claim Objections

Claims 4-8, 14-18, and 24-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter:

Re claims 4, 14, and 24, the prior art fails to disclose or suggest "disabling the SMI timer if throttling is disabled; and enabling the SMI timer is throttling is enabled".

Re claims 5, 15, and 25, the prior art fails to disclose or suggest "updating the throttling state if the access is a write; and returning the throttling state if the access is a read".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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